Effective Post-Programming Screening of Antifuse FPGAs for Space Applications

Yasuo Sakaide, Kimiharu Kariu, Kenji Numata, Akihisa Tsukino, Mikihiko Urano, Kenichi Chiba, Kenji Sugimoto, Yoshihisa Tsuchiya, Toshifumi Arimitsu

High-Reliability Components Corporation

Y. Sakaide

Abstract

For a decade, HIREC has been working for post-programming screening of antifuse FPGAs and supplying the FPGAs to Japanese space customers, meeting with the full technical satisfactions.

In this paper, we report the results on the effectiveness of the post-programming screening for antifuse FPGAs to ensure the reliable use of the FPGAs.

Introduction of HIREC

HIREC

is a test house qualified by JAXA (Japan Aerospace Exploration Agency)

- **quality assurance (surveillance, source inspection, etc.)**
- **screening and quality conformance inspection**
- **environmental test (radiation test, etc.)**
- **Destructive physical analysis, construction analysis and failure analysis (SEM inspection, etc.) for semiconductor devices (MPU, Gate Array, Memory, etc.) for space applications.**

performs design of semiconductor devices for space application.

- **design (MPU, Memory, FPGA, etc.)**

1. Purpose of post-programming screening

(1) Post-Programming Electrical Parameter Test (PPEPT)

To ensure the electrical parameters as a built configuration.

Because:

Actual delay parameters cannot be measured for blank devices.

Programming instruments doesn't assure the electrical performance (i.e. functionality, timing, and so forth) in full operating range.

PPEPT is necessary for programmed antifuse FPGAs.

(2) Post-Programming Dynamic Burn-In (PPDBI)

To screen the potential damage to internal logic elements during device programming.

Because:

High programming voltage (Vpp) may damage the internal logic elements.

Dynamic burn-in is the most effective way to exercise all the active elements as a built configuration.

PPDBI is necessary for programmed antifuse FPGAs.

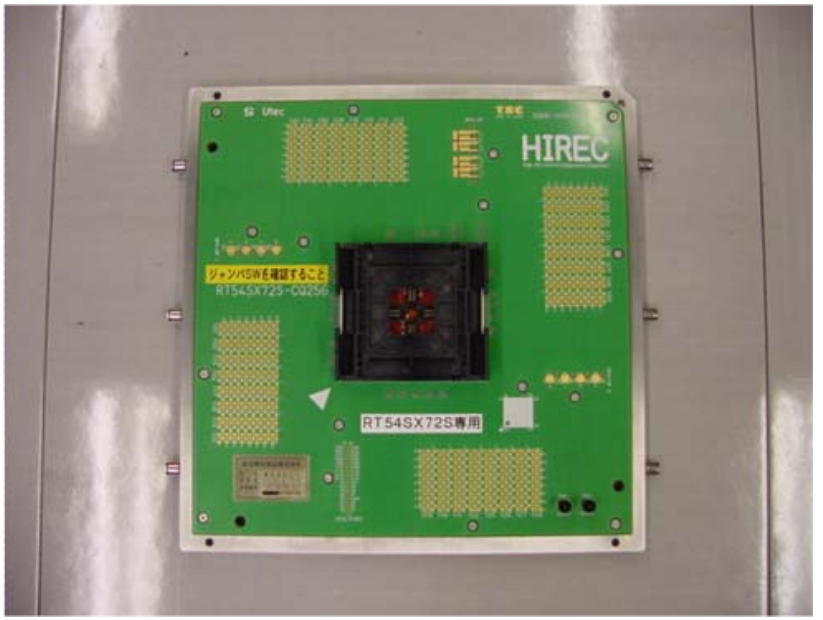
HIREC Post-programming screening flow

HIREC Class Ⅰ Flow	HIREC Class Ⅱ Flow
Pre Burn-In Electrical Parameters Test at +25ºC (1)(2)	Pre Burn-In Electrical Parameters Test at +25ºC (1)
Dynamic Burn In +125ºC, 240hrs	Dynamic Burn-In +125ºC, 160hrs.
Interim (Post Burn-In) Electrical Parameters Test at +25ºC (2)(4)	N/A
Delta Calculation Percent Defective Allowable(PDA)(3)(4)	N/A
Static Burn-In at +150ºC, 72hrs(4)	N/A
Final Electrical Parameters Test at +25ºC (2)	Final Electrical Parameters Test at +25ºC (2)
Delta Calculation, Percent Defective Allowable(PDA)(3)	Delta Calculation, Percent Defective Allowable(PDA)(3)
Final Electrical Parameters Test at -55ºC, +125ºC (2)	Final Electrical Parameters Test at -55ºC, +125ºC (2)
External Visual	External Visual

Notes: (1) Pre Burn-In electrical parameters tests are measured for Subgroup 1, 7, and 9.
(2) Interim (Final) electrical parameters tests are measured for Subgroup 1, 7 and 9(1,2,3,7,8,9 and 10) listed on MIL-PRF-38535, TableⅢ.
(3) Delta calculation is performed for the parameters specified in SMD.
(4) Option.

Electrical parameters test system in HIREC

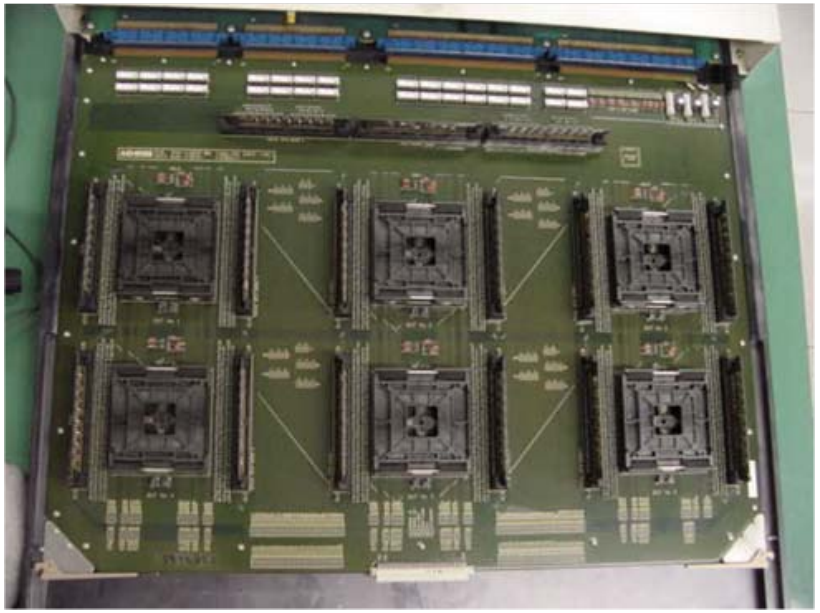
LSI test system



An example of DUT board

Dynamic burn-in test system in HIREC

Full dynamic burn-in system



An example of burn-in board

2. Results of post-programming screening

Post-programming screening summary performed in HIREC

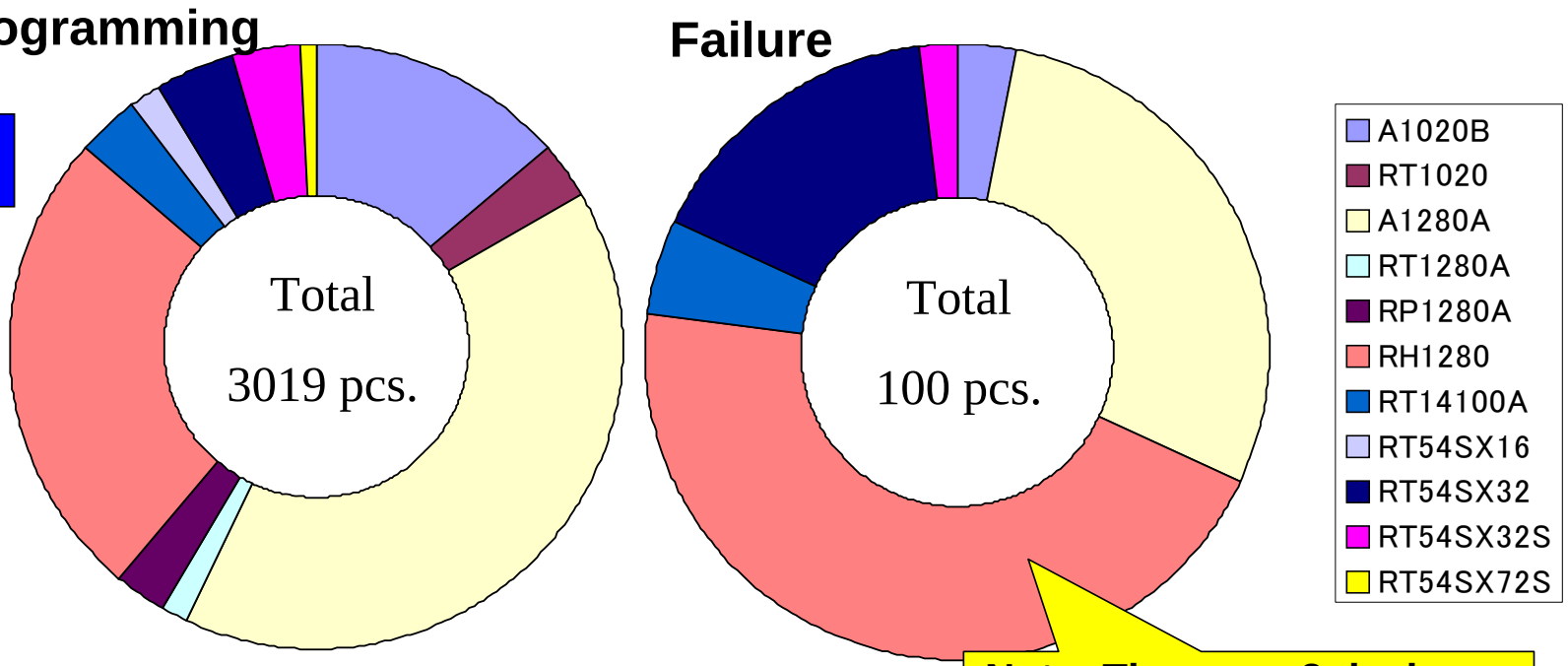
Product	Package	IN	OUT (Pass)	Test Item/Number of Failures or Issues																
				(1)	(2)			(3)	(4)			(5)	(6)					(7)		
				Programming	Pre Burn-In PPEPT			PPDBI	Final PPEPT (at +25ºC)			Delta Calculation	Final PPEPT					Others		
													125ºC				-55ºC	Issues of electrical		
					(a)	(b)	(c)	(c)	(a)	(c)	(e)	(a)	(b)	(c)	(d)	(e)		(a)	(b)	(e)
A1020B	CQ84	410	405	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	0
RT1020	CQ84	91	91	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A1280A	CQ172	1214	1176	29	0	1	1	1	0	0	1	0	0	0	0	0	0	3	0	0
RT1280A	CQ172	47	46	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RP1280A	CQ172	79	75	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0
RH1280	CQ172	766	715	45	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	1
RT14100A	CQ256	99	89	5	1	0	1	0	0	0	0	0	0	3	0	0	0	0	0	0
RT54SX16	CQ256	50	45	0	0	0	0	0	1	0	0	3	1	0	0	0	0	0	0	0
RT54SX32	CQ256	126	102	16	1	0	3	0	0	0	0	0	0	0	4	0	0	0	0	0
RT54SX32S	CQ256	109	104	2	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RT54SX72S	CQ256	28	28	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Total		3019	2876	100	6	3	5	2	1	0	1	4	1	3	4	1	0	3	2	1

Note: The numbers from (1) to (7) are related to those of following presentation.

(a)～(e) means fail mode on electrical parameters as shown below;
(a)・・・Standby supply current (IDD(STB))
(b)・・・Input leakage current (IIL/IIH)
(c)・・・Functional Test (FT) (“Functionality” only for PPDBI)
(d)・・・Output voltage (VOL/VOH)
(e)・・・All parameters

2. Results of post-programming screening (cont.)

(1) Programming



Summary of programming performed in HIREC

Note: There are 2 designs whose number of failures exceeded the maximum number of allowed programming failures defined by the manufacturer.

(2) Pre burn-in electrical parameters test at 25ºC by LSI tester.

Standby supply current (IDD(STB))

RP1280A (1pc.)
RT14100A (1pc.)
RT54SX32 (1pc.)
RT54SX32S (3pcs.)

Input leakage current (IIL/IIH)

A1280A (1pc.)
RP1280A (1pc.)
RH1280 (1pc.)

Functional test (FT)

A1280A (1pc.)
RT14100A (1pc.)
RT54SX32 (1pc.)

- **The instruments cannot ensure the quality/reliability of programmed FPGAs.**

(3)Post-Programming Dynamic Burn-In (PPDBI)

Anomaly of Functionality and Operating current during burn-in

A1280A (1pc.)
RH1280 (1pc.)

(4)Final electrical parameters test at 25 ºC

Standby supply current
RT54SX16 (1pc.)

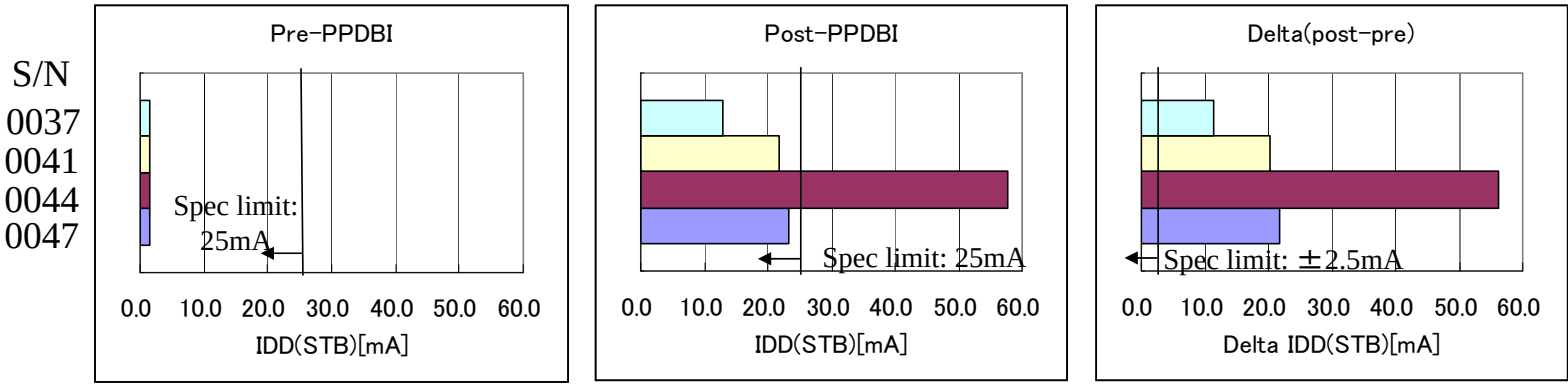
Catastrophic damage
A1280A (1pc.)

(5) Delta calculation

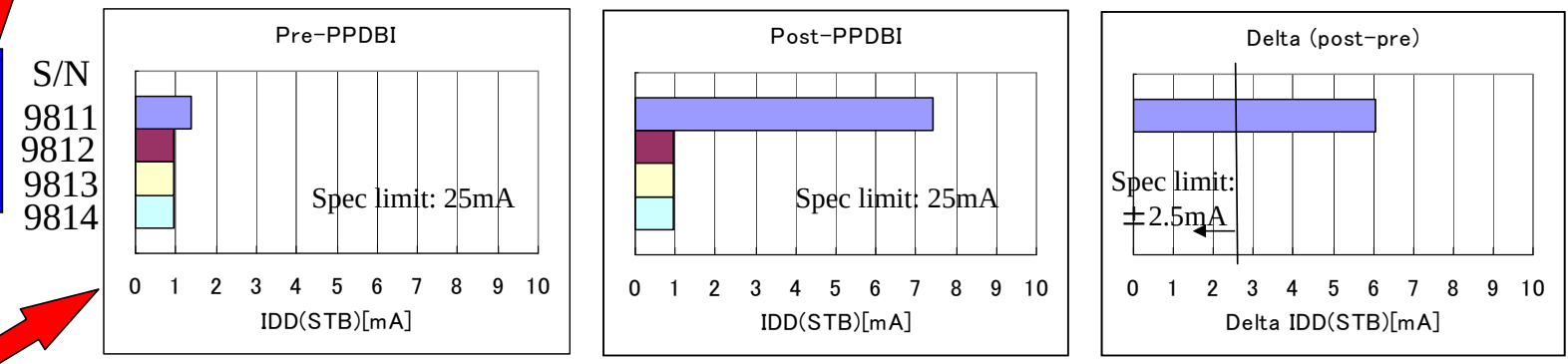
Standby supply current

RT54SX16 (3pcs.)
RH1280 (1pc.)

Anomalous delta for IDD(STB) for the same designed RT54SX16 (4pcs. from 4pcs.)



Anomalous delta for IDD(STB) for the same designed RH1280 (1pcs. from 4pcs.)



(6) Final electrical parameters test at -55 and +125ºC

Input leakage current (IIH)
RT54SX16
(1pc.)

Functional test (FT)
RT14100A
(3pcs.)

Output voltage (VOH)
RT54SX16
(4pcs.)

All parameters
RP1280A (1pc.)

S/N 2061 failed the input leakage current (IIL/IIH) at +125ºC for the same designed RP1280A

S/N	Pin No.	IIL[μA] Ta (°C)			IIH[μA] Ta (°C)			Notes
		−55	+25	+125	−55	+25	+125	
2054	131	−0.01	0.00	0.00	0.00	0.00	0.09	(1) OVER means range over in measurement. (2) Max Limits:±10[μA]
	132	0.00	0.00	0.00	0.00	0.00	0.08	
	137	0.00	0.00	0.00	0.00	0.00	0.08	
2061	131	0.00	0.00	OVER	0.00	0.00	82.8	
	132	0.00	0.00	140	0.00	0.00	OVER	
	137	0.00	0.00	30.4	0.00	0.00	OVER	

4. Conclusion

The post-programming screening has revealed that some portion of the antifuse FPGAs were defective after programming.

The schedule and costs might be strongly affected, if the above problems are discovered on the FPGAs embedded in the flight hardware.

The post-programming screening for antifuse FPGAs is mandatory for space applications.