New SET Characterization Technique Using SPICE for Fully Depleted CMOS/SOI Digital Circuit

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Abstract

The new SET characterization technique for 0.15 μm Fully Depleted CMOS/SOI digital circuits was investigates using SPICE and TCAD simulations. The SPICE simulation with a switch can readily reproduce the corresponding SET voltage response for a certain LET. This technique is valid as an alternative in all load and complementary transistor conditions, irrespective of the presence of a plateau region in the SET current waveform generated in a struck transistor.