Radiation Hardness-By-Design Library for a 0.15-μm Fully Depleted SOI-ASIC

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Abstract

This paper presents the Total Ionizing Dose and Single Event Effect test results on the improved Radiation Hardness-By-Design Library for a 0.15-μm Fully Depleted CMOS/SOI-ASIC fabricated by a commercial foundry. Sufficient immunity was demonstrated for TID and SEU/SET to meet requirements for space applications.

1. Introduction

Application-specific integrated circuits (ASICs) are a technology essential to achieving high-performance electronic systems for space applications. For the past 10 years, Radiation Hardness-By-Design (RHBD) techniques have often been used to develop ASICs for a harsh space environment, instead of the traditional methods, like the use of specialized radiation-hardened manufacturing processes developed specifically for space applications [1].

It is expected that Single Event Latchup (SEL) never occurs in SOI devices due to the non-existence of the parasitic p-n-p-n Silicon-Controlled Rectifier (SCR). Additionally, the Single Event Transient (SET) signals caused by heavy ions and high-energy protons in SOI devices are smaller as compared with those in equivalent bulk devices because of the lower sensitive volume. Although an SOI transistor still involves the parasitic bipolar transistor, which amplifies the collected charge and degrades SEU/SET immunity [2-3], the SEU/SET effects are relatively smaller than in bulk technologies. In 2006, we started to develop a standard logic cell library for a 0.15-μm Fully Depleted CMOS/SOI ASIC. The library conforms to commercial foundry design rules of a Fully Depleted SOI (FDSOI) device available from OKI Semiconductor Co., Ltd in Japan. One can easily obtain radiation-hardened low-power high-density ASICs for space applications using this standard cell library.

All the transistors are electrically isolated by dielectric material in SOI technologies; therefore, it is possible to realize the SET-free logic [5][6], which eliminates SET signal generation at output terminals using the circuit technique in conjunction with SOI technologies. This technique was used for the RHBD library. In our previous work in 2009 [4], we presented the initial Total Ionizing Dose (TID) and Single Event Effect (SEE) test results on the RHBD library. For TID immunity, it was demonstrated that this process had sufficient immunity up to 1 kGy(Si) inherently, according to the high dose rate test. For SEU/SET immunity, some SEUs were observed in RHBD latches and FFs at an Liner Energy Transfer (LET) of 64 MeV/(mg/cm^2). These SEUs can be eliminated by a slight change of the latch and FF circuits, where conventional inverters used for the internal clock buffers are replaced by SET-free inverters and the spacing between the redundant transistor pairs in the SET-free inverter is increased. The changes were applied to the RHBD library and SEE immunity was improved.

2. Characteristics of 0.15μm CMOS/SOI-ASIC

Table I summarizes the characteristics of the 0.15-μm CMOS/SOI RHBD ASIC. The process used is from OKI semiconductor in Japan.

In our previous works on RHBD SOI design [4-6], we proposed an optimized RHBD methodology, where SET-free inverters were applied only for memory elements in the sequential logic cells, not for combinational logic cells. Therefore, an SOI-ASIC standard cell library is constructed with the conventional (non-radiation-hardened) combinational logic cells, RHBD clock buffers, and RHBD sequential logic cells (latches and FFs with a scan path circuit).

The schematic diagram of the SET-free inverter [4-6] and the typical RHBD latch are illustrated in Fig. 1 (a) and (b). The SET-free inverter structure prevents SET pulse generation on its output in conjunction with SOI technology. The inverter loop in the RHBD latch is comprised of a SET-free inverter and a SET-free dynamic inverter. No SEU will be observed in the inverter loop itself because no SET pulse will be generated inside the

inverter loop. Additionally, as shown in Fig. 1 (b), the internal clock buffers in the latch were designed using SET-free inverters to prevent the bit flip caused by the ion strike on the off state transistors in the clock buffers.

On the layout of the SET-free inverter, the paired redundant transistors (Mp1-Mp2 and Mn1-Mn2) were placed with enough spacing to prevent a simultaneous upset by a single ion strike.

3. Radiation test

3.1 Test Chips

Three test chips have been designed for the SEU/SET immunity evaluation test. They contain a total of eight types of RHBD latches and four types of RHBD FFs, as shown in Table II. For these latches and FFs, the conventional inverters used for the internal clock buffers are replaced by SET-free inverters and the spacing between the redundant transistor pairs in the SET-free inverter is increased to improve SEU/SET immunity. Each latch and FF was constructed as a 2-kb (512 words by 4 bits) memory block.

All this effort for the radiation hardening design was made to improve SEU/SET immunity and we did not perform any particular design improvement such as annular gate structure for TID effect. The hardness for TID was improved by the optimization of the impurity profile in the transistors.

3.2 Low Dose Rate Total Ionizing Dose (TID)

The low dose rate TID test was performed using Co-60 at the Japan Atomic Energy Agency (JAEA) in Takasaki, Japan. Test chips were irradiated at room temperature under the worst case bias condition (V_{DD}(Core) = 1.65 V). Note that V_{DD}(IO) were not under the worst case condition (1.65 V instead of 3.6 V) due to the limitation of the functional design of the I/O buffers (no logic level conversion circuit) for the test chips. The dose rate was 3.6 Gy(Si)/hr (0.1 rad(Si)/sec) and the total dose level was 1.28 kGy(Si). Three out of four samples were biased and the fourth was unbiased during the irradiation test.

3.3 Single Event Effects (SEU/SET)

The SEU/SET cross-section of the latches and FFs was measured with mono-energetic ions obtained from the heavy-ion accelerator at JAEA. The characteristics of the ions used are shown in Table III. The ion fluence was > 1×10^7 ions/cm^2. The cross-sections were measured with minimum V_{DD} of 1.35 V at room temperature, with a normal incidence angle for the ion strike in static mode, i.e., specific data were written before irradiation and read back after completion of the irradiation.

SEU is a result of capturing SET pulse using latches or FFs. To identify the location where SET signals are generated, the logic state at the data input terminal is inverted or non-inverted compared to the stored logic state during irradiation. In the non-inverted case (0_SAME and F_SAME), the logic state at the data input terminals of the latches or FFs is the same as the stored state in them. Any SEUs observed in this case are responsible for SET signals generated in the inverter loop in the latches or FFs. SEUs indicate that the charge sharing effect takes place between the redundant transistor pairs in the SET-free inverter. The cross-section for this type of SEU represents the inherent SEU immunity of the latches or FFs. In the inverted case (0_INV and F_INV), the logic state at the data input terminals is opposite to the stored state. In this case, the stored logic state is inverted if SET signals are propagated to the clock terminal of the latches or FFs, or generated in the clock gate inside them during irradiation. If SEUs are observed only in the inverted case, the latch or FF is inherently immune to SEUs, but is sensitive to SET signals propagated to or generated in the clock gate. Otherwise, if the latch or FF has a set or reset function, the meaning of the SAME condition and INV condition becomes a little complicated. When a latch or FF has a set function, the SET signals propagated to the set input terminal or generated in the set input related gates may cause additional SEUs in F_SAME and F_INV conditions. In cases with a reset function, the same thing also happens for the reset terminal.

4. Results and discussion

4.1 Low Dose Rate TID Response

Fig. 2 shows the TID response for the quiescent current (I_{CC}) during irradiation. The quiescent current showed no change up to 800 Gy(Si) at least. Although the current was slightly increased at a higher dose level, the functionality was not disrupted. As we mentioned in Section IIIA, the test chip was not utilize any hardening structure such as annular gate structure to improve TID immunity particularly. Therefore, the TID test result demonstrates that this commercial process has an inherent TID immunity of more than 1 kGy(Si). In order to improve the TID immunity, the TID shielding package is available as needed for the ASIC. The TID immunity of 10 kGy(Si) can be achieved by the package.

4.2 SEU/SET

Table IV (a), (b), and (c) show the SEU/SET counts and their cross-sections as a function of LET.

No SEUs were observed in almost all types of latches and FFs in SAME and INV conditions except LALSH and LALRH (Table IV (c)). This means that SET pulses were not generated in both the inverter loop and the

internal clock buffers, and they are inherently immune to SEUs. For LALSH and LALRH, a few Multiple Bit Upsets (MBUs) were observed in F_INV and F_SAME conditions. The MBUs were up to 16-bit errors in the same Y address line. Therefore, the cause of MBUs is SET pulse propagation to the set or clock input terminal. The MBUs will be eliminated if the external circuits connected to the set and clock line are constructed using RHBD clock buffers, which are expected to never generate SET pulses on their output.

5. Conclusions

In this paper, we described the results of the radiation test including the low dose rate TID and SEU/SET on the improved RHBD library for the 0.15-μm Fully Depleted CMOS/SOI ASIC. For TID, it was demonstrated that the ASICs fabricated with this library were immune up to 1 kGy(Si), despite no particular hardening effort being made for TID effects. The TID shielding package is available as needed for the ASIC, therefore, the TID immunity of 10 kGy(Si) can be achieved by the package. For SEU/SET, no SEUs were observed in RHBD latches and FFs at an LET up to 64 MeV/(mg/cm^2), although a few MBUs responsible for the external buffers were observed. The MBUs will be eliminated using the RHBD clock buffers for the external circuits. The improved RHBD library is now available for actual space applications with the 0.15-μm Fully Depleted CMOS/SOI process. Some projects in Japan are ongoing using this RHBD library.

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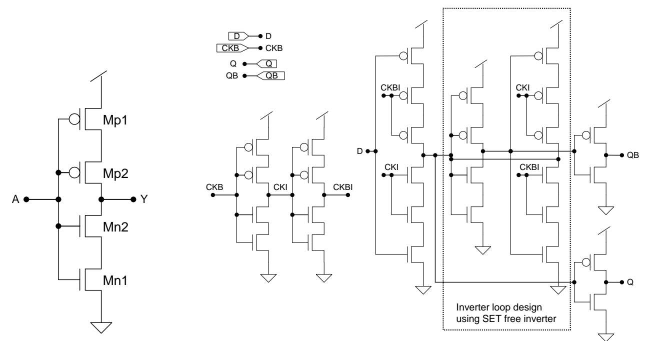
TABLE I RHBD 0.15-μm SOI-ASIC Characteristics

Parameters	0.15μm Fully Depleted SOI-ASIC	Notes
Standard Cells	Low Consumption type (Normal V_{th}) High Speed type (Low V_{th})	-42 type of RHBD sequential logic cells, -293 type of combinational logic cells (including RHBD clock buffers)
IOs	Input/Output/Bidirectional digital IOs PCI, LVDS	Under development
Special Cells	1P SRAM PLL	Under development
Supply Voltage	3.3V I/O / 1.5V Core	
Power Consumption (Stand-by Operation)	0.5378 μW (Low Consumption type) 0.0473 μW (High Speed type)	
Gate Delay	43ps (Low Consumption type) 33ps (High Speed type)	@25 degree C
Usable Gate (max)	5.6MGate (2NAND equivalent)	Die size ~100mm^2
Metal Structure	6 Metal Layers	
Usable Package	304pinCQFP, 352pinCQFP	Radiation Shielded Package



(a) SET-free inverter (b) Typical RHBD latch

Fig. 1 Schematic diagram of (a) SET-free inverter and (b) Typical RHBD latch

TABLE II RHBD Latch/FF Cells Tested

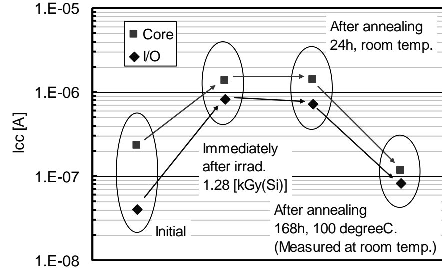
Test Chip	Cell Type V_{th}	Type	Drive	Symbol	Memory Block Capability
#1	N[*1]	RHBD F/F	xH	FFNH	2Kbit(512w4b)
	N	RHBD F/F with Reset	xH	FFNRH	2Kbit(512w4b)
	N	RHBD F/F with Set	xH	FFNSH	2Kbit(512w4b)
	N	RHBD F/F with Set/Reset	xH	FFNSRH	2Kbit(512w4b)
#2	N	RHBD Gated Latch	xH	GLNH	2Kbit(512w4b)
	N	RHBD Gated Latch with Set	xH	GLNSH	2Kbit(512w4b)
	N	RHBD Latch with Set/Reset	x1	LANSR1	2Kbit(512w4b)
	N	RHBD Latch with Set/Reset	x2	LANSR2	2Kbit(512w4b)
#3	L[*2]	RHBD Latch	xH	LALH	2Kbit(512w4b)
	L	RHBD Latch with Reset	xH	LALRH	2Kbit(512w4b)
	L	RHBD Latch with Set	xH	LALSH	2Kbit(512w4b)
	L	RHBD Latch with Set/Reset	xH	LALSRH	2Kbit(512w4b)

[*1] Normal V_{th}
[*2] Low V_{th}

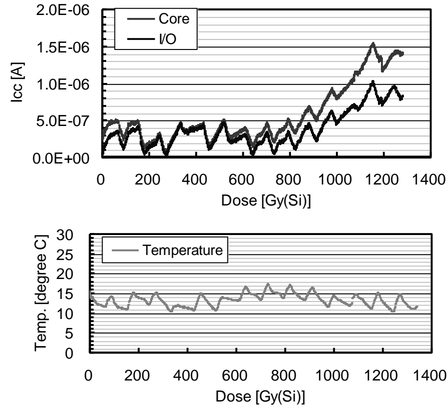
TABLE III Characteristics of Heavy Ion Species (JAEA[*1]@Takasaki, Japan)

Element Symbol	Energy [MeV]	LET [MeV/(mg/cm²)]	Range [μm]
Ne	69.7	6.5	39.0
Ar	137	15.2	36.1
Kr	289	40.8	37.3
Xe	393	64.0	34.6

[*1] JAEA: Japan Atomic Energy Agency



(a) Icc at pre-irradiation, immediately after the irradiation test, after annealing for 24 hr, and after annealing at 100 deg. C for 168 hr



(b) Icc and temperature during the irradiation test

Fig. 2 Quiescent Current for Core (I_{CC}) versus TID during the low dose rate test; (a) Icc at pre-irradiation, immediately after the irradiation test, after annealing for 24 hr, and after annealing at 100 deg. C for 168 hr, (b) Icc and temperature during the irradiation test.

TABLE IV (a) SEU Test Results of Four Types of RHBD Normal V_{th} D-type F/F

Ion	LET	Data State	Fluence [particles/cm²]	# of Error FFNSRH	FFNH	FFNSH	FFNRH	Cross Section [cm²/bit] FFNSRH	FFNH	FFNSH	FFNRH
Xe	64	F_INV	3.23E+07	0	0	0	0	<1.51E-11	<1.51E-11	<3.02E-11	<1.51E-11
		0_INV	3.26E+07	0	0	0	0	<1.50E-11	<1.50E-11	<2.99E-11	<1.50E-11
		F_SAME	3.59E+07	0	0	0	0	<1.36E-11	<1.36E-11	<2.72E-11	<1.36E-11
		0_SAME	3.26E+07	0	0	0	0	<1.50E-11	<1.50E-11	<2.99E-11	<1.50E-11

"<" means no SEUs were observed.

TABLE IV (b) SEU Results of Two Types of RHBD Normal V_{th} Gated Latch and Two Types of RHBD Normal V_{th} Latch with Different Drivability

Ion	LET	Data State	Fluence [particles/cm²]	# of Error LANSR2	GLNH	LANRS1	GLNSH	Cross Section [cm²/bit] FFNSRH	FFNH	FFNSH	FFNRH
Xe	64	F_INV	2.20E+07	0	0	0	0	<2.22E-11	<2.22E-11	<4.43E-11	<2.22E-11
		0_INV	2.46E+07	0	0	0	0	<1.98E-11	<1.98E-11	<3.96E-11	<1.98E-11
		F_SAME	1.12E+07	0	0	0	0	<4.34E-11	<4.34E-11	<8.69E-11	<4.34E-11
		0_SAME	1.26E+07	0	0	0	0	<3.88E-11	<3.88E-11	<7.76E-11	<3.88E-11

"<" means no SEUs were observed.

TABLE IV (c) SEU Results of Four Types of RHBD Low V_{th} Latch

Ion	LET	Data State	Fluence [particles/cm²]	# of Error LALSRH	LALH	LALSH	LALRH	Cross Section [cm²/bit] LALSRH	LALH	LALSH	LALRH
Xe	64	F_INV	1.16E+07	0	0	2[*1]	0	<4.21E-11	<4.21E-11	8.43E-11	<4.21E-11
		0_INV	1.11E+07	0	0	0	0	<4.41E-11	<4.41E-11	<8.82E-11	<4.41E-11
		F_SAME	1.16E+07	0	0	1[*1]	1[*1]	<4.20E-11	<4.20E-11	4.20E-11	4.20E-11
		0_SAME	1.24E+07	0	0	0	0	<3.94E-11	<3.94E-11	<7.88E-11	<3.94E-11
Kr	40.8	F_INV	1.24E+07	0	0	0	0	<3.93E-11	<3.93E-11	<7.87E-11	<3.93E-11
		0_INV	1.26E+07	0	0	0	0	<3.88E-11	<3.88E-11	<7.76E-11	<3.88E-11
		F_SAME	1.25E+07	0	0	0	0	<3.91E-11	<3.91E-11	<7.81E-11	<3.91E-11
		0_SAME	1.23E+07	0	0	0	0	<3.98E-11	<3.98E-11	<7.96E-11	<3.98E-11

[*1] Error counts of Multiple Bit Upsets (1 MBU error means up to 16 bits SEU in the same Y address)