Optimization for SEU/SET Immunity on 0.15 ㎛ Fully Depleted CMOS/SOI Digital Logic Devices

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Outline

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2. HBD Design Circuitry
3. Experimental
4. Results and Discussion
5. Conclusion

Introduction

◆Sensitive volume for charge collection =
CMOS/bulk technology > CMOS/SOI technology

However, CMOS/SOI technologies are not inherently hard against SEEs because of the parasitic effects !!

→ Parasitic bipolar effects
→ Anomalous charge collection in the drain regions

◆Single-Event Transients (SETs) signal generation is .....

- unavoidable in CMOS/bulk technologies.
→ All the transistors are isolated by the reverse biased p-n junctions.

- avoidable in CMOS/SOI technologies.
→ All the transistors are electrically isolated by dielectric material.

Therefore, it is possible to eliminate the SET signal generation by implementing circuit design (**Hardness-By Design**) techniques with SOI technologies.

◆The objective of this work is .....

- To design the SEU/SET immune circuit using SET-free logic circuit and optimize the mitigation technique with minimum penalties for speed, power and area with Fully Depleted (FD) SOI technology.

◆Targeted process

- OKI's 0.15 μm FDSOI commercial process
- Test chips comprised of SET-free logic circuits were fabricated.

◆Evaluation

- Heavy ion irradiation test (@JAEA[*1]) for SEU observation
- 2D Device simulation (TCAD) for SET generation
- Circuit simulation (SPICE) for SET propagation

[*1] JAEA : Japan Atomic Energy Agency

HBD Design Circuitry

OKI's 0.15µm FDSOI commercial process

Table 1. Fabrication process

	OKI (FD-SOI)
Wafer	UNIBOND wafer
Substrate	P-Sub
Metal Layers	1 Poly / 5 Metals
Drawn Gate Length	0.15㎜
Top Silicon Thickness	40nm
Buries Oxide Thickness (BOX)	200nm
Isolation Technology	LOCOS*
Supply Voltage	1.0V ± 10%

*** LOCOS : Local Oxidation of Silicon**

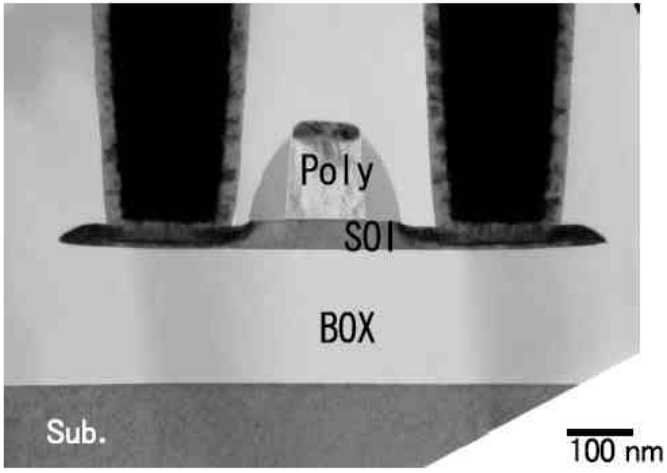
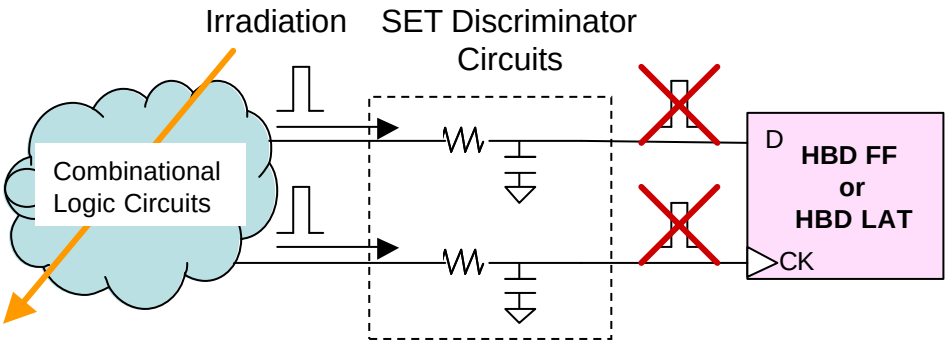


Fig.1 Cross Section of 0.15µm FDSOI Transistor by TEM
(Photo from OKI Technical Journal, 196, Vol. 70, No.4, Oct. 2003, pp.60-63)

How to eliminate errors caused by SET signals??

(1) The use of SET signal discriminators that ignore the unexpected short pulse at input terminals

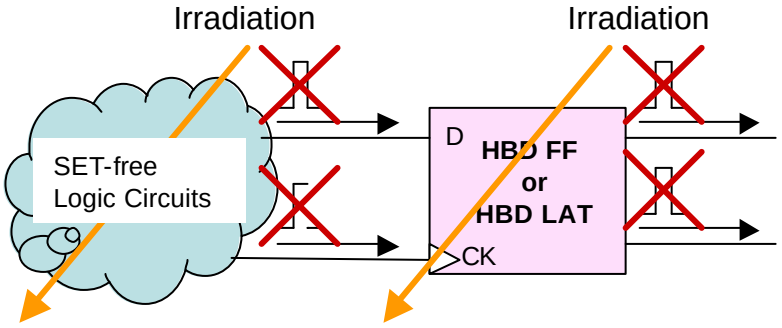
→Bulk technology
(Because of unavoidable of SET pulse generation)



Limitation of the maximum operation frequency caused by the SET discriminators.

(2) The use of SET-free logic circuits that never generate SET signals at their output

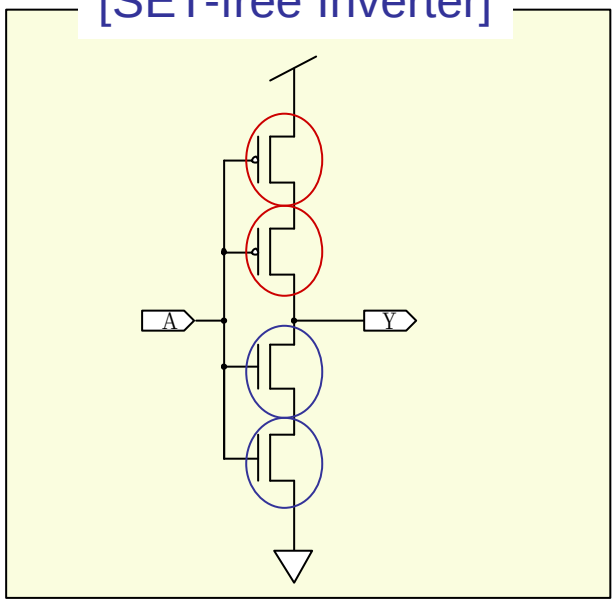
→SOI technology



Expectation to achieve a breakthrough in the operation frequency.

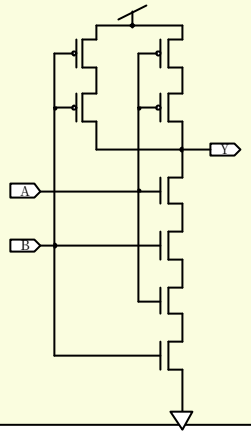
What is SET-free logic circuit??

[SET-free Inverter]

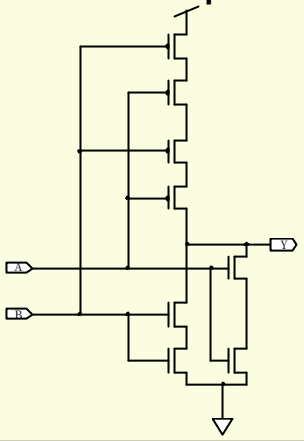


[HBD Combinational Logic]

SET-free 2-Input NAND

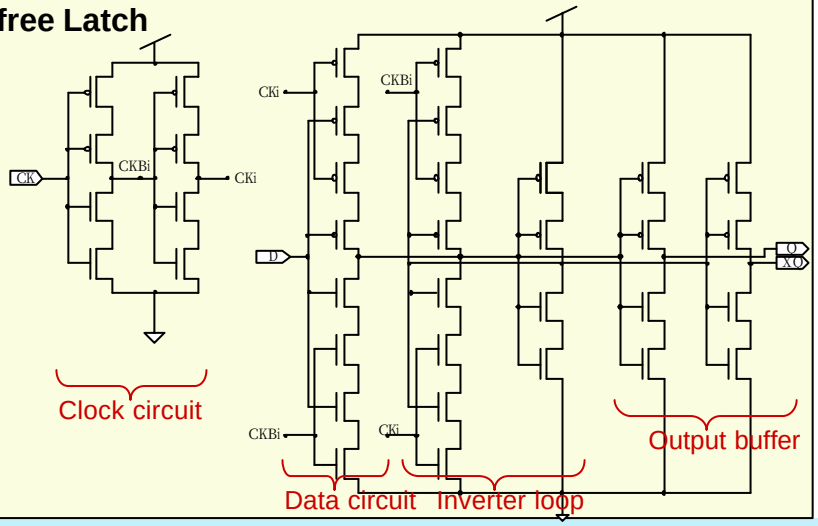


SET-free 2-Input NOR



[HBD Sequential Logic]

SET-free Latch

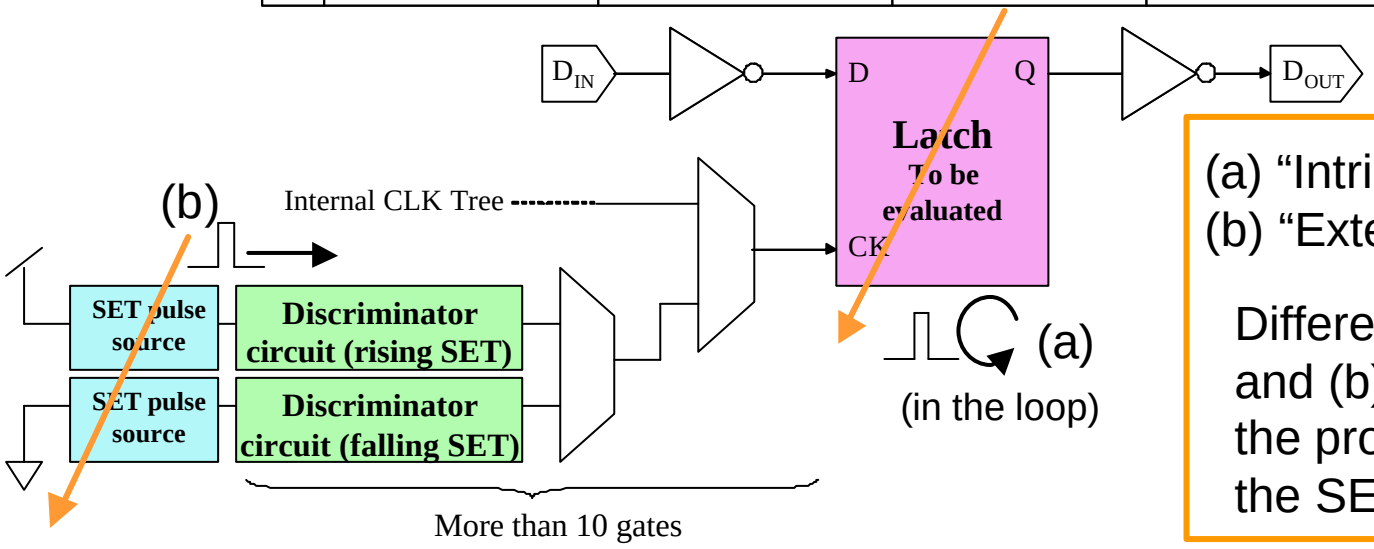


Applied bias voltage is shared with redundant pair transistors. If one of the redundant transistors is struck by the incident particle, the applied voltage is transferred to another transistor with slight displacement current only.

Design for test chip

~~Combination of the test elements~~

#	SET pulse source	INV-DLY in Discriminator circuit	Latch to be evaluated	SRAM Block
1	Conventional inverter	INV-DLY3	Latch with INV-DLY2	512-bit
2	4Tr Inverter	INV-DLY3	Latch with INV-DLY2	512-bit
3	6Tr Inverter	INV-DLY3	Latch with INV-DLY2	512-bit
4	8Tr Inverter	INV-DLY3	Latch with INV-DLY2	512-bit
5	Conventional inverter	INV-DLY1	Latch with INV-DLY2	512-bit
6	6Tr Inverter	INV-DLY1	Latch with INV-DLY2	512-bit

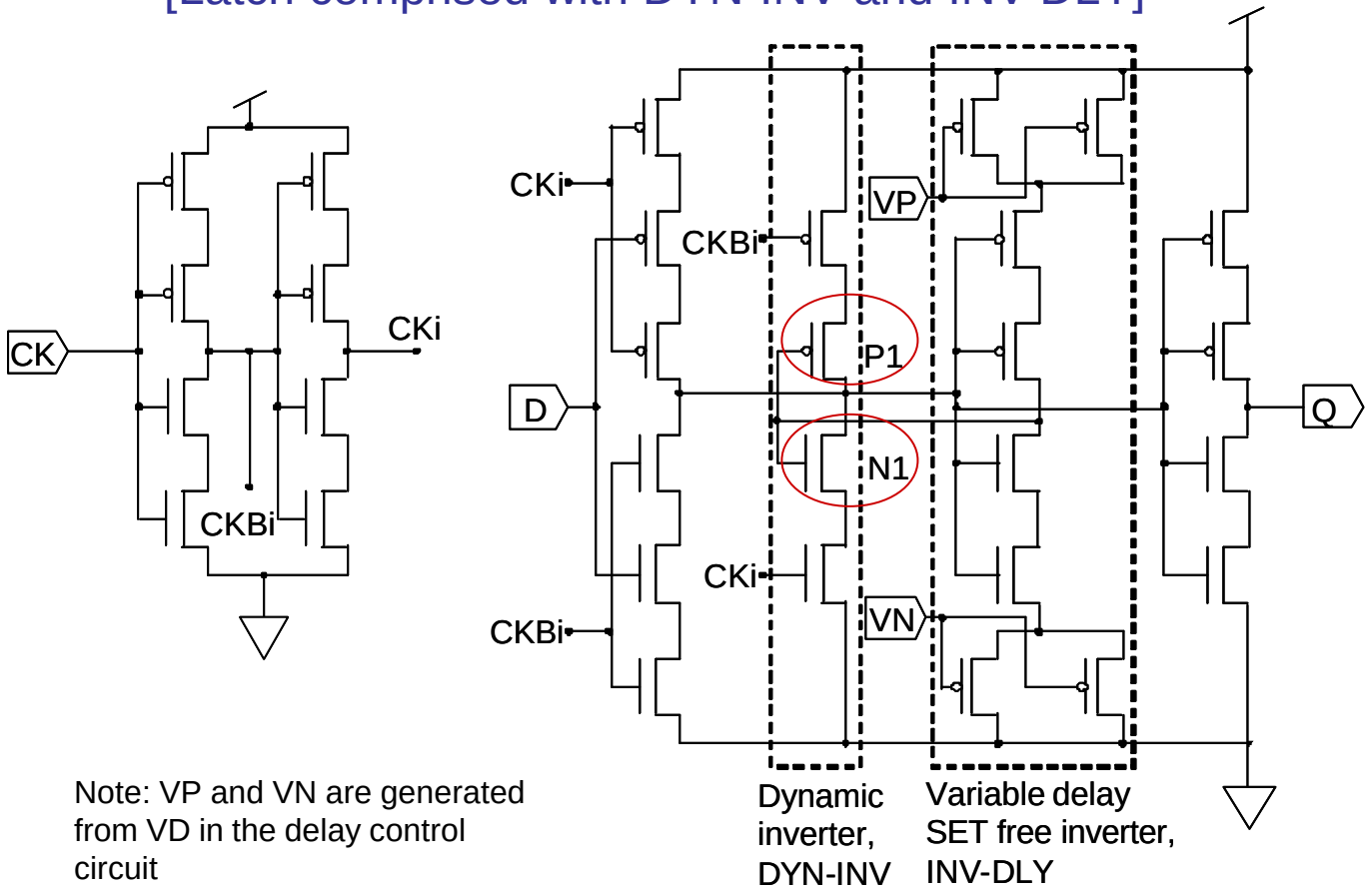


(a) “Intrinsic” mode SEUs
(b) “External” mode SEUs

Difference between (a) and (b) is attributable to the propagation path for the SET pulse.

Latch to be evaluated

[Latch comprised with DYN-INV and INV-DLY]



Note: VP and VN are generated from VD in the delay control circuit

- SEU will be triggered when off state transistors (P1 and N1) in DYN-INV are struck with ions.

- SEU rate can be reduced as the delay time of INV-DLY increased.

Experimental

Experimental Condition

~~Characteristics of ions used~~

Element Symbol	Energy [MeV]	LET [MeV/(mg/cm^2)]	Range [μm]
Ne	69.7	6.54	39.0
Ar	137	15.18	36.1
Kr	289	40.80	37.3
Xe	393	64.00	34.6

In Japan Atomic Energy Agency (JAEA)

SEU Test Condition

- V_{DD} : 0.9V (minimum V_{DD})
- Temp. : Room Temperature
- Procedure : Static Mode

(Step 1)
- "Intrinsic" mode SEUs

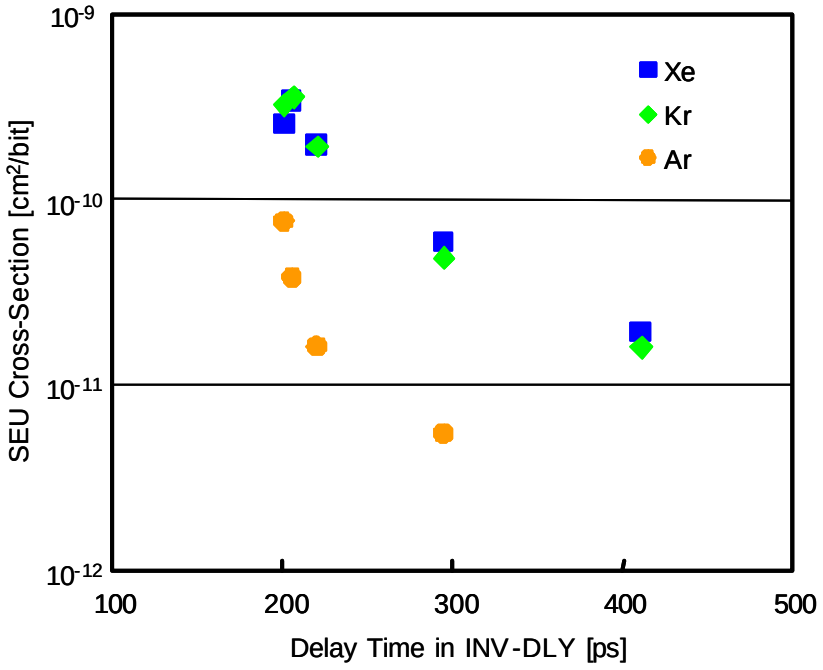
→The measured SEU cross-sections are caused by ions hitting a transistor P1 or N1 in the latch to be evaluated. And from this result, we know the delay time to eliminate the SEUs originated these transistors.

(Step 2)
- "External" mode SEUs

→The measured SEU cross-sections are originated with SET pulse propagated to the clock terminal.

Results and Discussion

Heavy ion irradiation test
"Intrinsic" mode SEUs



"Intrinsic" mode SEU cross-sections as a function of delay time in INV-DLY measured with Xe, Kr, and Ar.

(1) No SEUs were observed with Ne ion.

(2) SEUs observed were only originated with a transistor N1 in the latch ("H" to "L" inversion).

(3) SEUs were observed up to 300 ps delay time of INV-DLY with Ar irradiation and up to 400 ps with Kr and Xe irradiation.

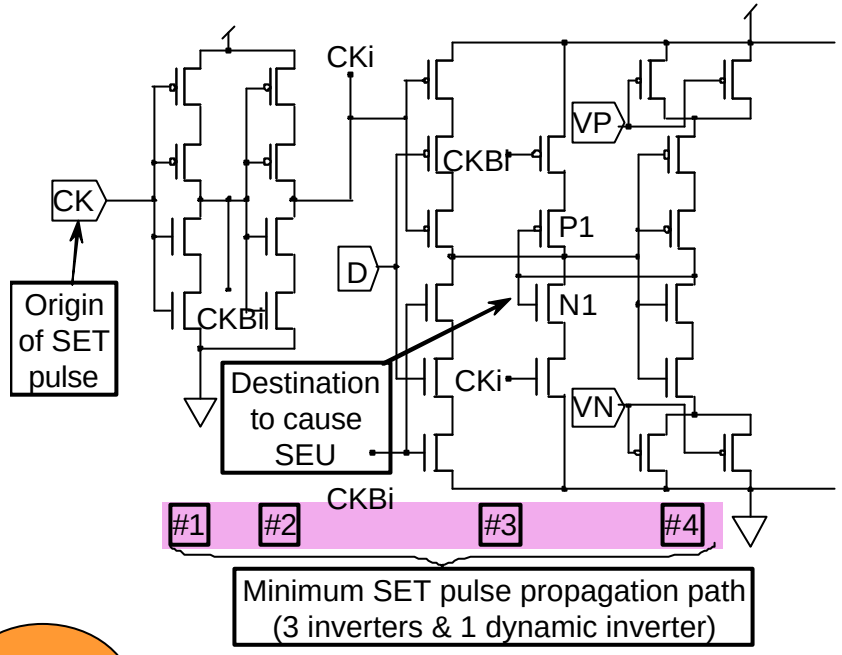
→ The width of SET pulses is shorter for Ar ions compared with Kr and Xe ions.

Heavy ion irradiation test
"External" mode SEUs

(4) SEUs were NOT observed with all the ion and SET pulse source combinations with the delay time setting of INV-DLY to eliminate "intrinsic" mode SEUs.

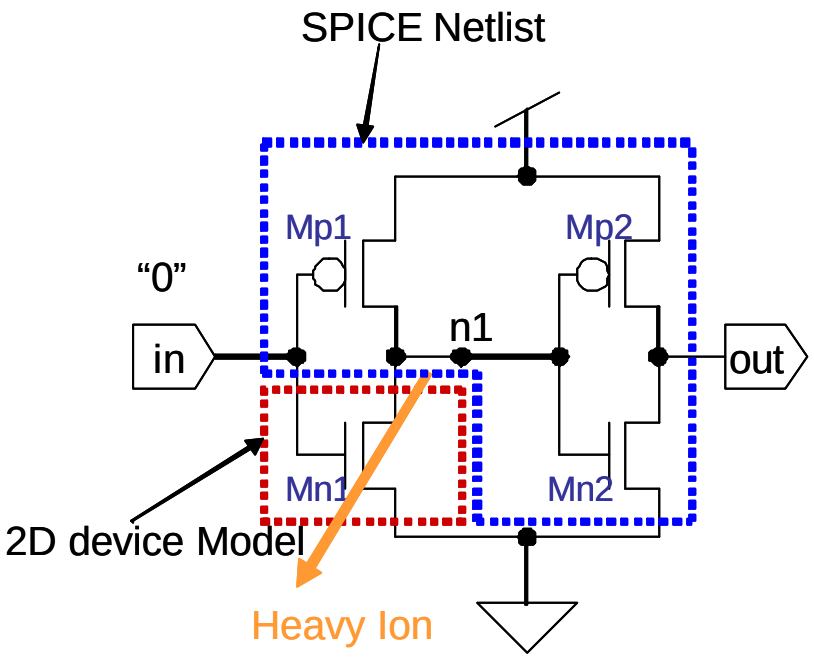
→ SET pulses generated in the device have the amplitude and width to propagate just 1 SET-free inverter or so, but disappear after passing through 4 or more SET-free inverters and dynamic SET-free inverter?????

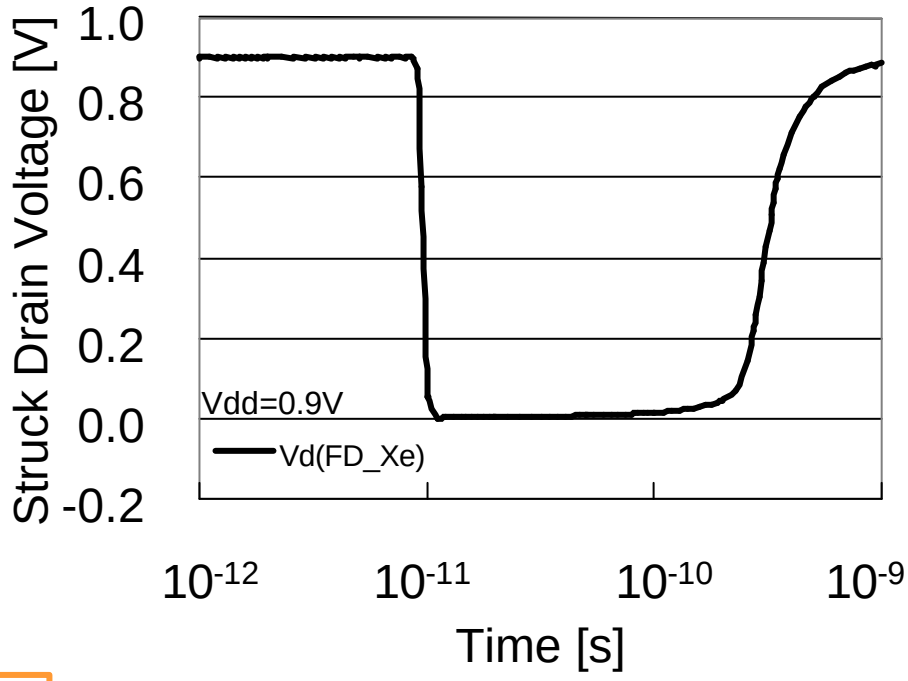
[Latch comprised with DYN-INV and INV-DLY]



Simulation was performed to confirm this hypothesis.

Device simulation (TCAD) for SET generation

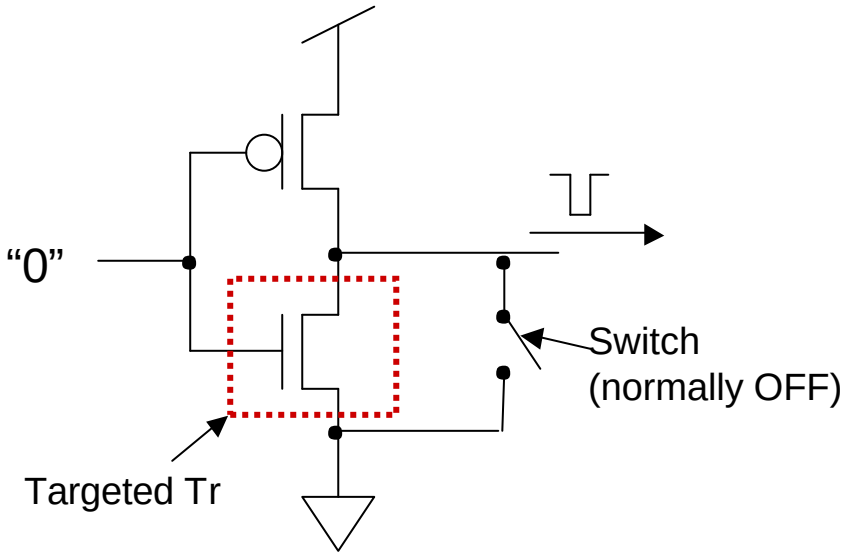


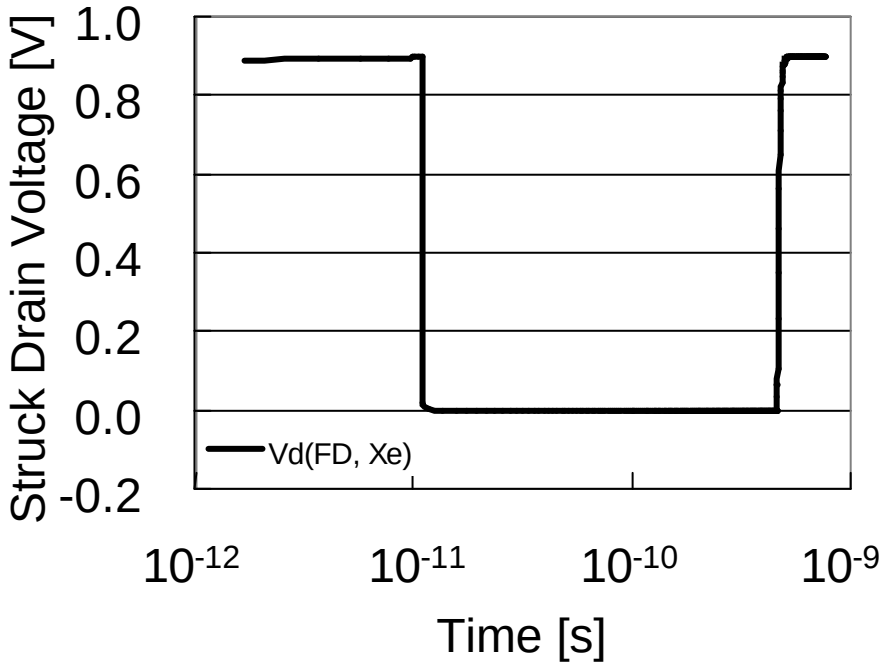


Simulated circuit for 2-D mixed mode device simulation using Synopsys TCAD. OFF state N channel transistor, Mn1 is a source of SET pulse generated by heavy ions.

SET pulse response simulated by **TCAD** with LET of 64.0 MeV/(mg/cm^2) for FDSOI.
The collected charge calculated from drain current of Mn1 was 24.2 fC.

SPICE simulation for SET propagation(1)



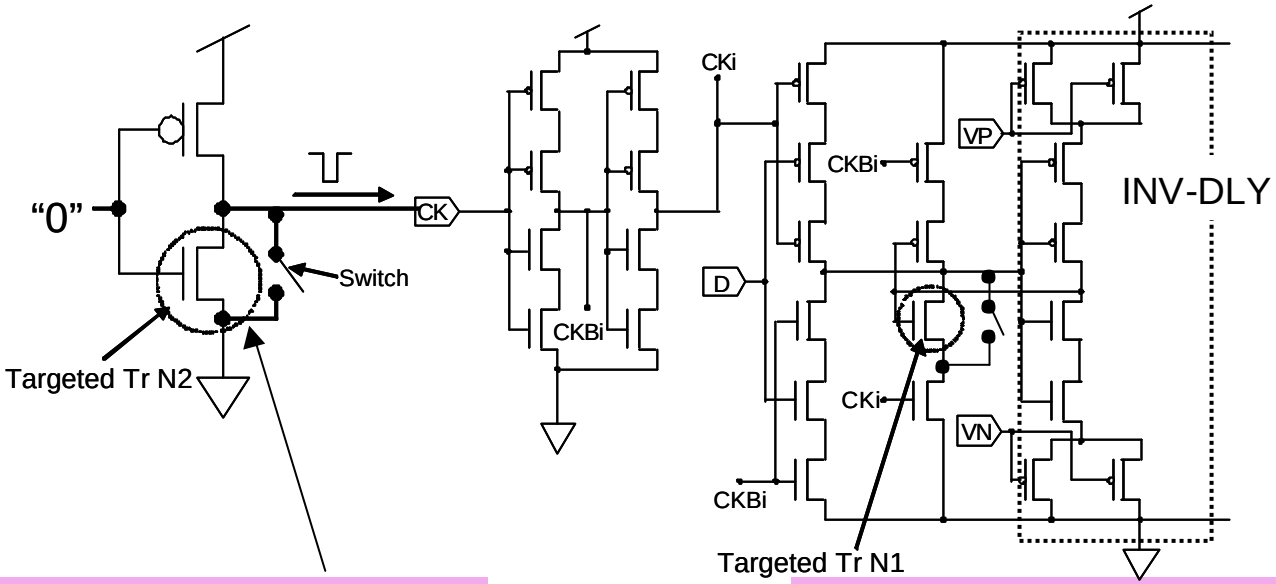


The drain voltage response by TCAD can be simulated easier with the SPICE simulator, provided the collected charge is given from the device simulation by TCAD.

SET pulse response simulated by **SPICE** with LET of 64.0 MeV/(mg/cm^2)(Xe ion) for FDSOI. SPICE simulation was performed applying the specific value of the collected charge (24.2 fC).

SPICE simulation for SET propagation(2)

When the collected charge of 24.2 fC (Xe ion) was injected.....



"External" mode SEUs

No SEUs were observed even if INV-DLY was set the minimum delay time.

→Good agreement with the experimental result!!

"Intrinsic" mode SEUs

SEUs were observed when INV-DLY was set up to 400 ps delay time.

→Good agreement with the experimental result!!

Conclusion

(1) The experimental and simulation results clearly demonstrated that the SET pulses generated in the FDSOI were completely attenuated with several stages of the gate, even if the devices were struck with Xe ions having an LET of 64.0 MeV/(mg/cm^2) because “external” mode SEUs were prevented.

(2) It means that it is possible to utilize the conventional (non-SET-free) combinational logic cells even just in front of the input terminal of the HBD sequential circuits.

(3) There are considerable penalties for speed, power and area to utilize the SET-free logic circuit for the all combinational and sequential logic cells, even if SET-free logic structure is effective for SEU/SET with FDSOI.

(4) Therefore, the hardening technique to utilize non-SET free combinational logic cells and hardened sequential logic cells significantly optimizes these penalties with the inherent SET immunity of FDSOI technology.